

IN THE CLAIMS:

Please note that all claims currently pending and under consideration in the referenced application are shown below. This listing of claims will replace all prior versions and listings of claims in the application.

Please cancel claim 10 without prejudice or disclaimer.

Please amend claims 1, 4, 8, 13, 33, 45 and 46 as set forth below.

Listing of Claims:

1. (Currently Amended) A method for aligning a semiconductor device package with a carrier substrate for electrical interconnection therebetween, the method comprising: forming at least two channels through the semiconductor device package from a first major surface thereof to a second, opposing major surface thereof; providing a major surface of the carrier substrate with at least two alignment features including forming at least two holes in the carrier substrate, each of which are spaced and positioned in respective correspondence to one of the at least two channels; forming at least one of the at least two pins with a mechanical self-locking mechanism proximate at least one end thereof; carrying the at least two pins with a head of a pick and place device, engaging the at least two channels formed in the semiconductor package with at least two pins ~~carried by a head of pick and place device~~ and grasping the semiconductor package with the pick and place device; positioning the pick and place device and the semiconductor device package over the carrier substrate with the first major surface of the semiconductor package facing the major surface of the carrier substrate; aligning the at least two pins with the at least two alignment features of the carrier substrate; and placing the at least two pins through the at least two channels and into the at least two holes; and engaging a portion of a second, opposing surface of the carrier substrate with the mechanical self-locking mechanism.

2-3. (Canceled)

4. (Currently Amended) The method of ~~claim 1~~ claim 13, wherein forming the at least two holes in the carrier substrate includes forming at least two blind holes therein.

5. (Canceled)

6. (Previously presented) The method of claim 1, further comprising forming the at least two pins of an electrically non-conductive material.

7. (Previously presented) The method of claim 1, further comprising forming the at least two pins of an anti-static material.

8. (Currently Amended) The method of ~~claim 1~~ claim 13, further comprising affixing the at least two pins to both the semiconductor device package and to the carrier substrate.

9. (Withdrawn) The method of claim 8, wherein affixing the at least two pins to the semiconductor device package and to the carrier substrate includes thermally bonding the pins to at least one of the semiconductor device package and to the carrier substrate.

10. (Cancelled)

11. (Previously presented) The method of claim 1, further comprising removing the at least two pins subsequent to the alignment of the at least two channels with the at least two alignment features.

12. (Cancelled)

13. (Currently Amended) ~~The method of claim 12, further comprising~~ A method for aligning a semiconductor device package with a carrier substrate for electrical interconnection therebetween, the method comprising:
forming at least two channels through the semiconductor device package from a first major surface thereof to a second, opposing major surface thereof;
providing a major surface of the carrier substrate with at least two alignment features including
forming at least two holes in the carrier substrate, each of which are spaced and
positioned in respective correspondence to one of the at least two channels;
engaging the at least two channels formed in the semiconductor package with at least two pins
carried by a head of pick and place device and grasping the semiconductor package with
the pick and place device;
positioning the pick and place device and the semiconductor device package over the carrier
substrate with the first major surface of the semiconductor package facing the major
surface of the carrier substrate;
aligning the at least two pins with the at least two alignment features of the carrier substrate;
placing the at least two pins through the at least two channels and into the at least two holes; and
releasing the at least two pins from the head of the pick and place device subsequent placing the
at least two pins through the at least two channels and into the at least two holes.

14 -19. (Cancelled)

20. (Withdrawn) The method of claim 1, wherein the at least two channels are each defined by a diameter and wherein the method further comprises forming at least one of the at least two channels with a larger diameter than that of at least one other channel of the at least two channels.

21. (Withdrawn) The method of claim 20, wherein providing the major surface of the carrier substrate with at least two alignment features includes correlating a size of each of the at least two alignment features with a size of a respectively corresponding channel of the at least two channels.

22. (Withdrawn) The method of ~~claim 1~~ claim 13, wherein forming the at least two channels includes forming the at least two channels in an asymmetrical pattern on the semiconductor device package.

23. (Withdrawn) The method of ~~claim 1~~ claim 13, wherein forming the at least two channels includes forming at least one notch on a periphery of the semiconductor device package.

24. (Previously presented) A method of testing a semiconductor device package having a plurality of discrete conductive elements disposed in a pattern on a surface thereof, the method comprising:

providing a carrier substrate having a plurality of terminal pads arranged in a pattern corresponding to a mirror image of the pattern of discrete conductive elements;

forming at least two channels in the semiconductor device package, each channel passing from a first surface thereof to a second, opposing surface thereof;

providing the carrier substrate with at least two alignment features including forming at least two holes in the carrier substrate, each of which are respectively spaced and positioned in correspondence to one of the at least two channels;

placing the semiconductor device package over the carrier substrate;

aligning each channel of the at least two channels formed in the semiconductor device package with a corresponding alignment feature of the at least two alignment features of the carrier substrate including placing pins formed of a non-conductive material through the at least two channels and into the at least two holes;

electrically contacting each discrete conductive element of the plurality with a terminal pad of the plurality;

passing at least one electrical signal between the semiconductor device package and the carrier substrate; and

removing the pins subsequent to the alignment of each of the at least two channels with a corresponding alignment feature of the at least two alignment features.

25-26. (Canceled)

27. (Previously presented) The method of claim 24, wherein forming at least two holes in the carrier substrate includes forming at least two blind holes.

28-29. (Canceled)

30. (Previously presented) The method of claim 24, further comprising forming the pins of an anti-static material.

31. (Previously presented) The method of claim 24, further comprising affixing the pins to both the semiconductor device package and to the carrier substrate.

32. (Previously presented) The method of claim 31, wherein affixing the pins to the semiconductor device package and to the carrier substrate includes thermally bonding the pins to at least one of the semiconductor device package and the carrier substrate.

33. (Currently Amended) The method of ~~claim 29~~ claim 24, further comprising forming a mechanical self-locking mechanism proximate at least one end of each pin.

34. (Canceled)

35. (Previously Presented) The method of claim 27, wherein placing the semiconductor device package over the carrier substrate includes using a pick and place device.

36. (Previously presented) The method of claim 35, wherein the pick and place device is used to align the semiconductor device package with the carrier substrate by carrying the pins with the head of the pick and place device and placing the pins through the at least two channels and the at least two holes.

37-42. (Canceled)

43. (Previously presented) The method of claim 24, wherein the at least two channels are each defined by a diameter and wherein the method further comprises forming at least one of the at least two channels with a larger diameter than that of at least one other channel of the at least two channels.

44. (Previously presented) The method of claim 43, wherein providing at least two alignment features on the carrier substrate includes correlating a size of each alignment feature of the at least two alignment features with a size of a corresponding channel of the at least two channels.

45. (Currently Amended) The method of ~~claim 25~~ claim 24, wherein forming the at least two channels includes forming the at least two channels in an asymmetrical pattern on the semiconductor device package.

46. (Currently Amended) The method of ~~claim 25~~ claim 24, wherein forming the at least two channels includes forming at least one notch on a periphery of the semiconductor device package.

47-62 (Canceled)